RazorCam: A Prototyping Environment for Video Communication

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1. INTRODUCTION

With the increasing complexity of embedded systems,in particular, of the embedded hardware/software systems for video applications, the trend is to perform the verification of components in the early stages of the design flow[3].The SystemC/TLM has emerged as the defacto standard for systems verification[4]. It includes dedicated description features and verification features, like constraint random stimulus generation for testbenches and functional coverage [4]; which makes it adequate for prototyping and verifying embedded systems.

Our focus in this work is to design generic embedded hardware /software architecture for video applications and to provide the symbolic representation to allow programmability and verification at a very high abstraction level.

Our main contributions are:

- ✓ To provide a holistic design flow for capturing computer vision applications at a higher abstraction -level with subsequent refinements and verification down to the hardware/software implementation.
- ✓ To derive a generic computing path and architecture for complex video applications.
- ✓ To design a viable FPGA embedded camera infrastructure for rapid prototyping.

In the rest of this work we present the main challenges, followed by the descriptionof our target system.

2. CHALLENGES

In this work,we present an integrated environment that will provide to designers of video applications, tools to implement, verify and evaluate their systems in a real environment. We propose a four-step design approach:

1. **System Specification**:Applications are specified in C/C++. OpenCV library [2] is used to define computer vision application behavior.
2. **High-level Hardware/Software system**: the initial application is partitioned intoHardware and Software tasks. OpenCV is used to implement the software parts. The hardware parts are described using SystemC [1]. Finally, the Transaction Level Modeling (TLM) [1] is used for high-level system verification (formal or functional) and simulation.
3. **Register-transfer-level**:The hardware parts (SystemC description) are translated into a RTL implementation (VHDL or Verilog).
4. **Emulation**:the RazorCam, runningLinux, is used to test the final system in a real-life environment.

The RazorCam, an FPGA-based embedded camera, allows designersto investigate various video applications without having to deal with low-level details of the hardware implementation.

3. TARGET SYSTEM

The target system is the RazorCam.The RazorCam is a smart camera system offering a flexible and extensible Hardware /software environment to prototype and to verify video applications. It is capable of streaming image data from 2 camera headboards, through a Spartan6-XC6SLX45 for processing and analysis. It offers a host of real world interfaces including uart and Ethernet connectivity. Linux is used as the embedded operating system on the microblaze (hard core inside FPGA) as it offers a solid, familiar platform for development with a feature-rich toolchain. The programmability and the seamless use of hardware accelerators in image processing application are insured through the design and implementation of a Streaming Data Interface (SDI). The Intel's OpenCV computer vision library has been ported to the system and is accessible in the Linux environment.

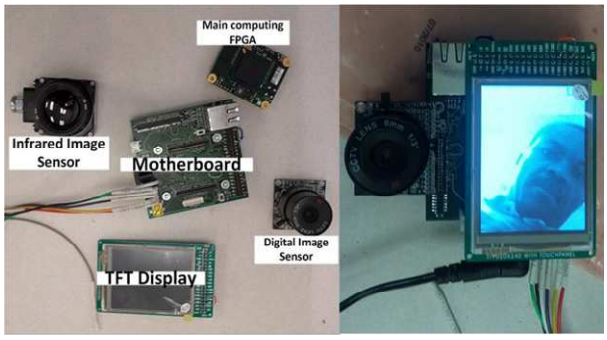

Figure 1: The target system

4. REFERENCES

[1] SystemC/TLM http://www.accellera.org/downloads/standards/systemc

[2] OpencCV,http://opencv.org/

[3]Giuseppe Di Guglielmo , GrazianoPravadelli, *A testbench specification language for SystemC verification*, Proceedings of the eighth IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis, October 07-12, 2012, Tampere, Finland.

[4]Marcio F.S. Oliveira , ChristophKuznik , Hoang M. Le , Daniel Große , Finn Haedicke , Wolfgang Mueller , Rolf Drechsler , Wolfgang Ecker , VolkanEsen, *The system verification methodology for advanced TLM verification*, Proceedings of the eighth IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis, October 07-12, 2012, Tampere, Finland.